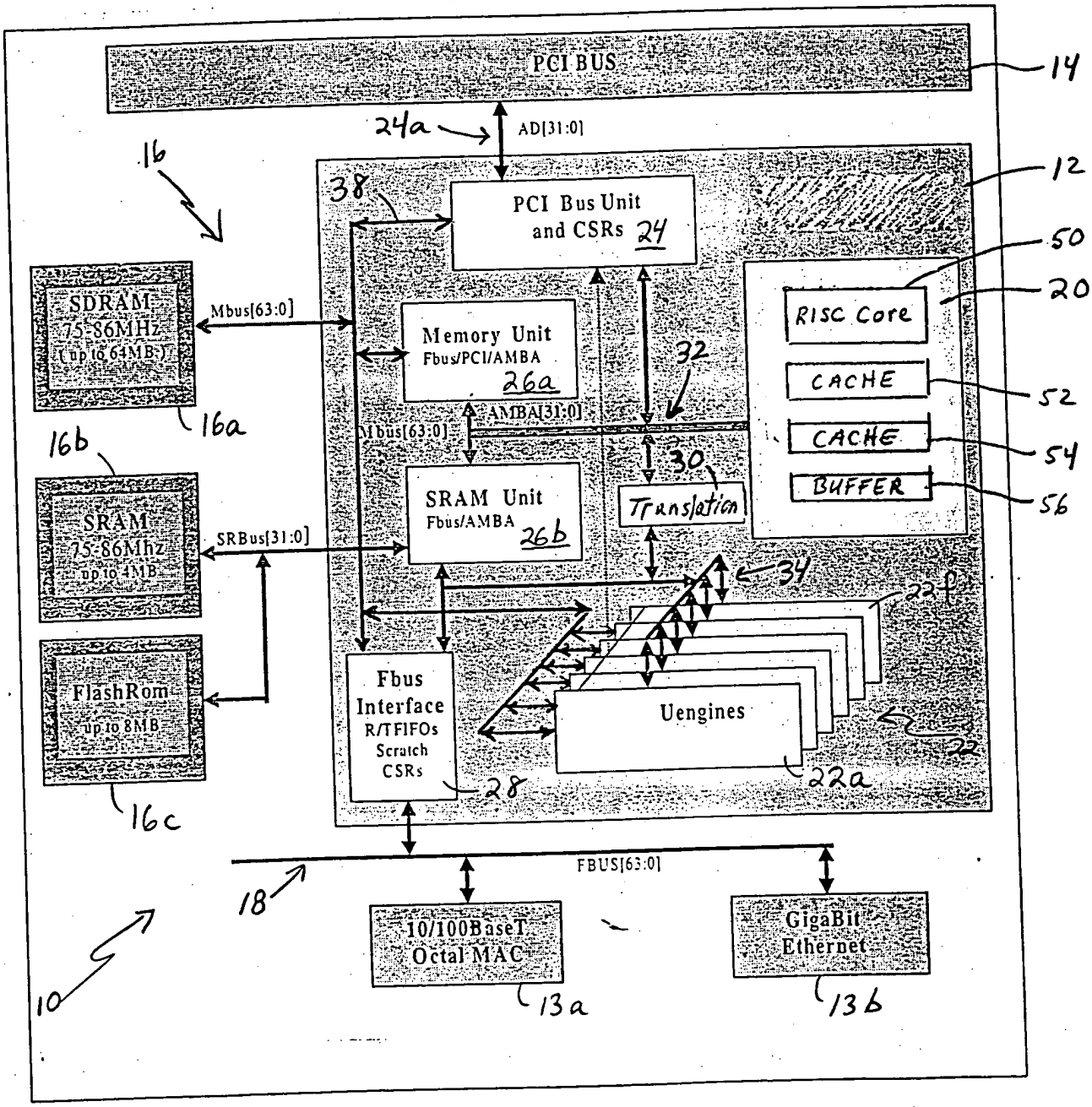


FIG. 1

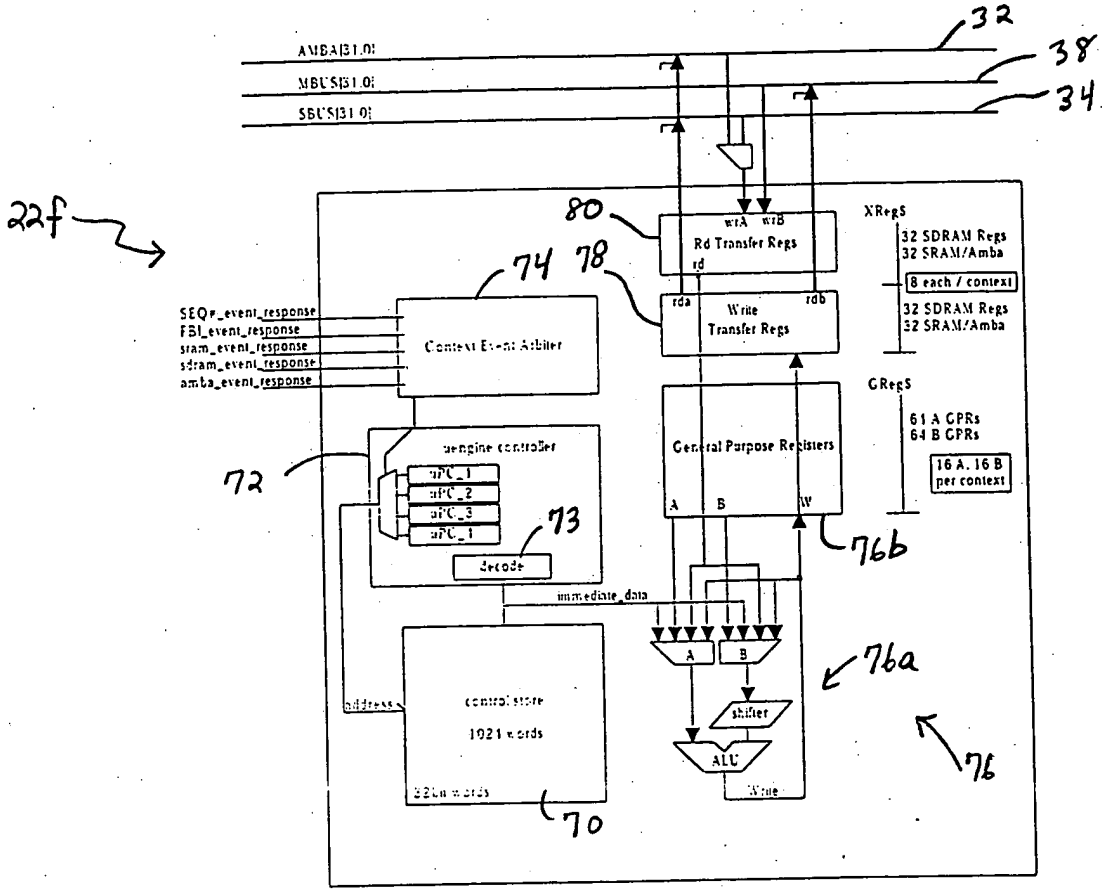
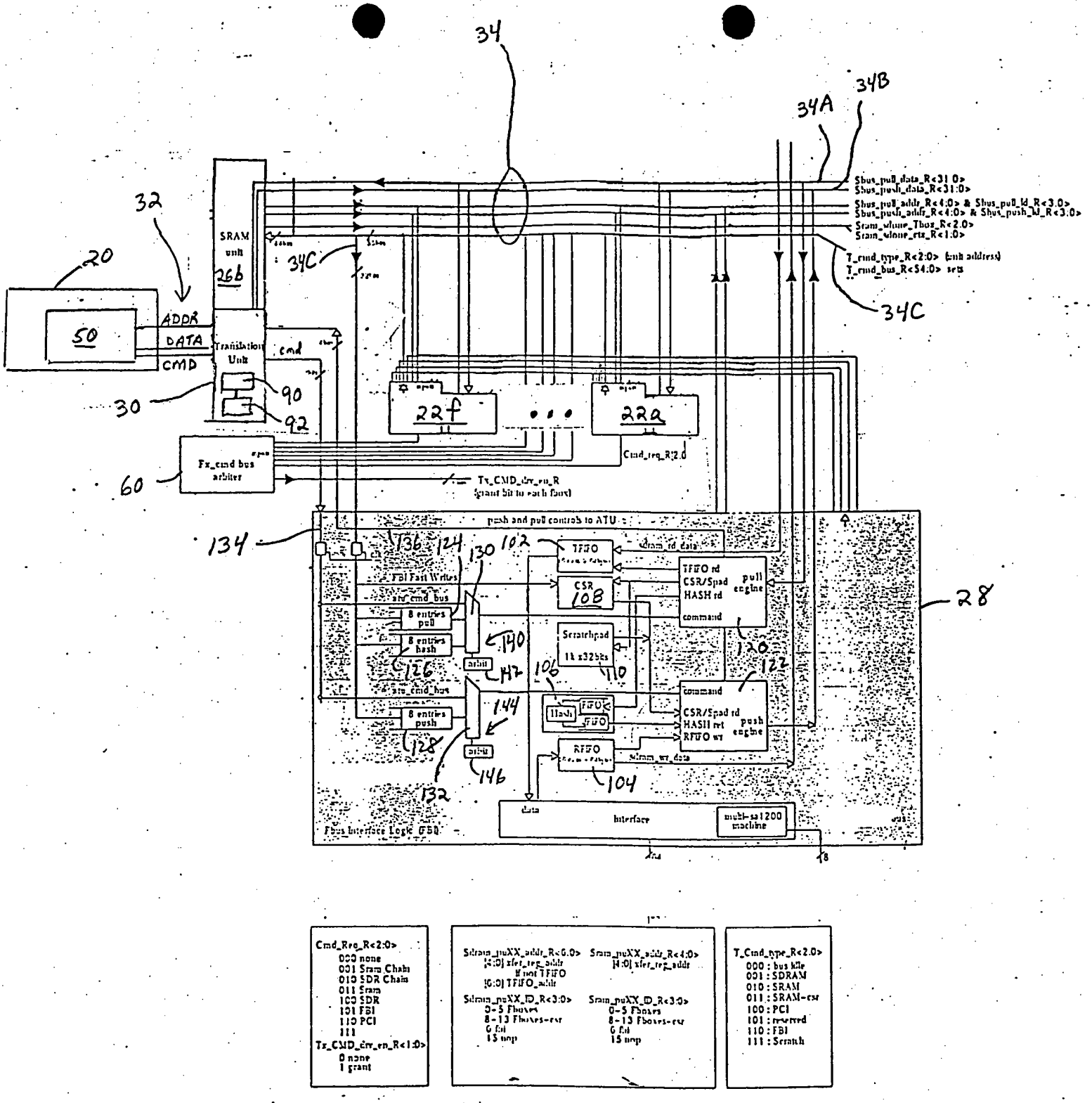


FIG. 2



Cmd_Req_R<2:0>
000 none
001 Sram Chain
010 SDR Chain
011 Sram
100 SDR
101 FBI
110 PCI
111
Tx_CMD_drv_en_R<1:0>
0 none
1 grant

Sram_puXX_addr_R<6:0>	Sram_puXX_addr_R<4:0>
[4:0] xfer_reg_addr	[4:0] xfer_reg_addr
if not TFIFO	
[6:0] TFIFO_addr	
Sram_puXX_ID_R<3:0>	**Sram_puXX_ID_R<3:0>**
0-5 Fbuses	0-5 Fbuses
8-13 Fbuses-esr	8-13 Fbuses-esr
6 fbi	6 fbi
15 ucp	15 ucp

T_Cmd_type_R<2:0>
000 : bus idle
001 : SDRAM
010 : SRAM
011 : SRAM-esr
100 : PCI
101 : reserved
110 : FBI
111 : Scratch

FIG. 3

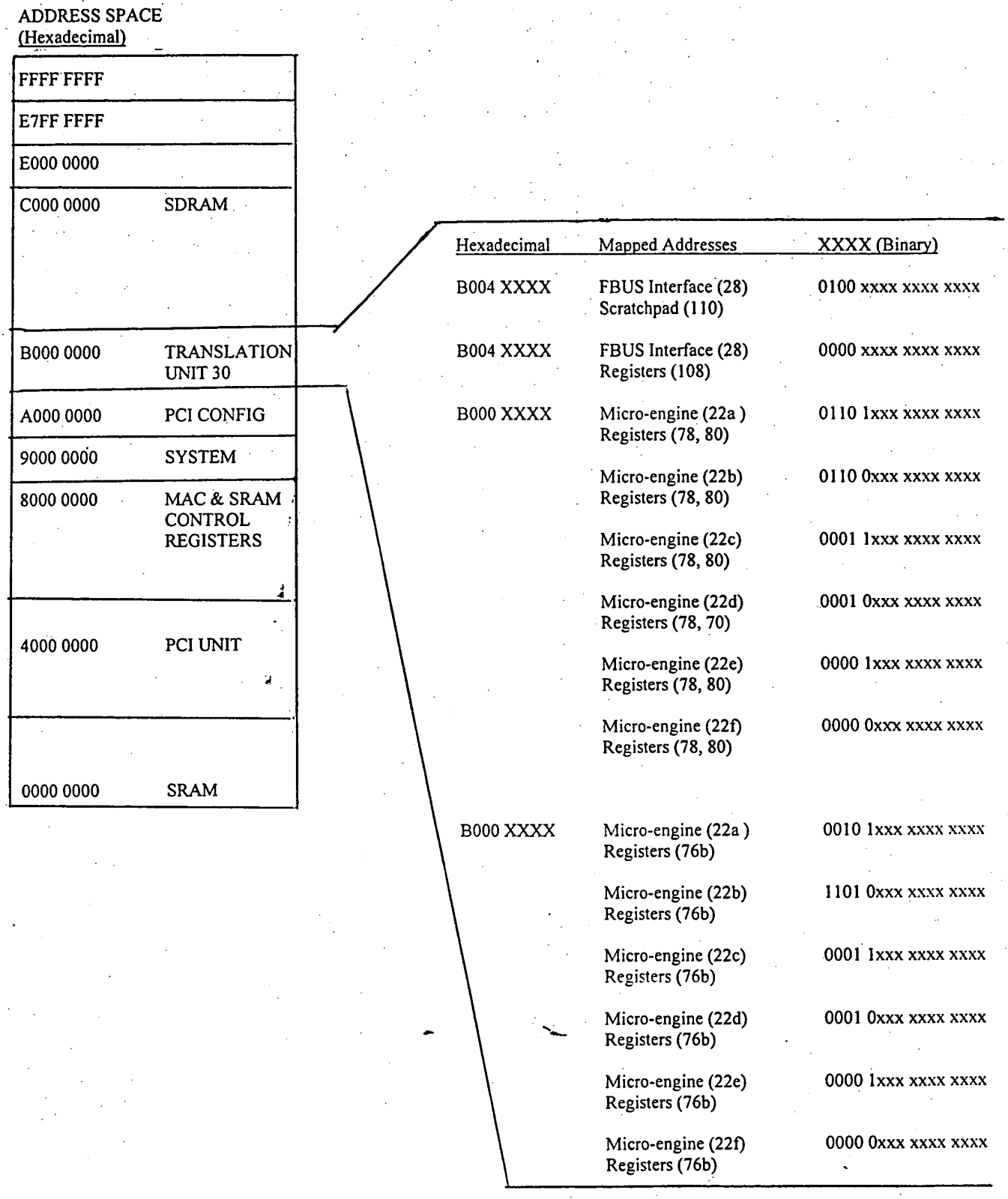


FIG. 4

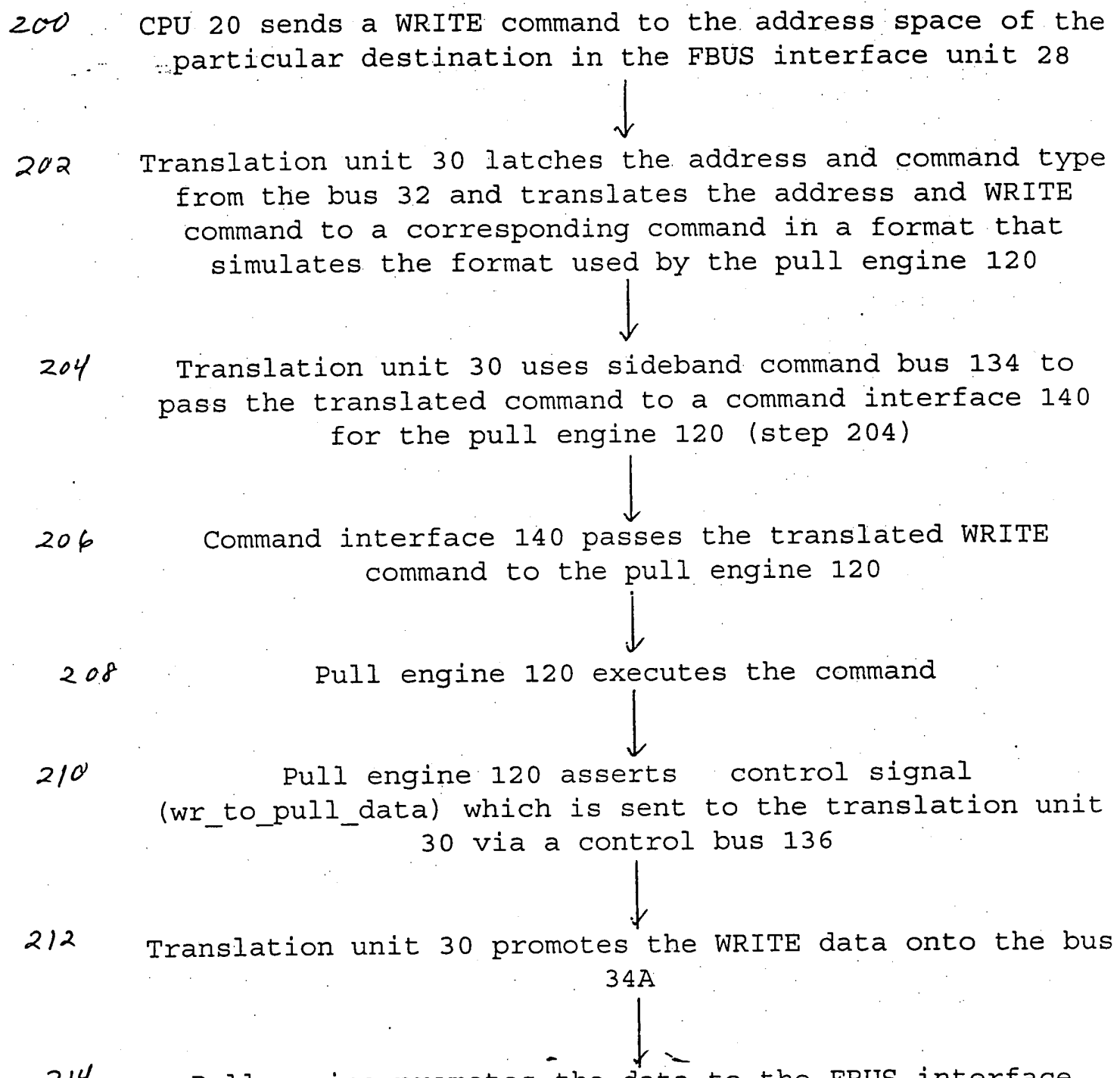


FIG. 5

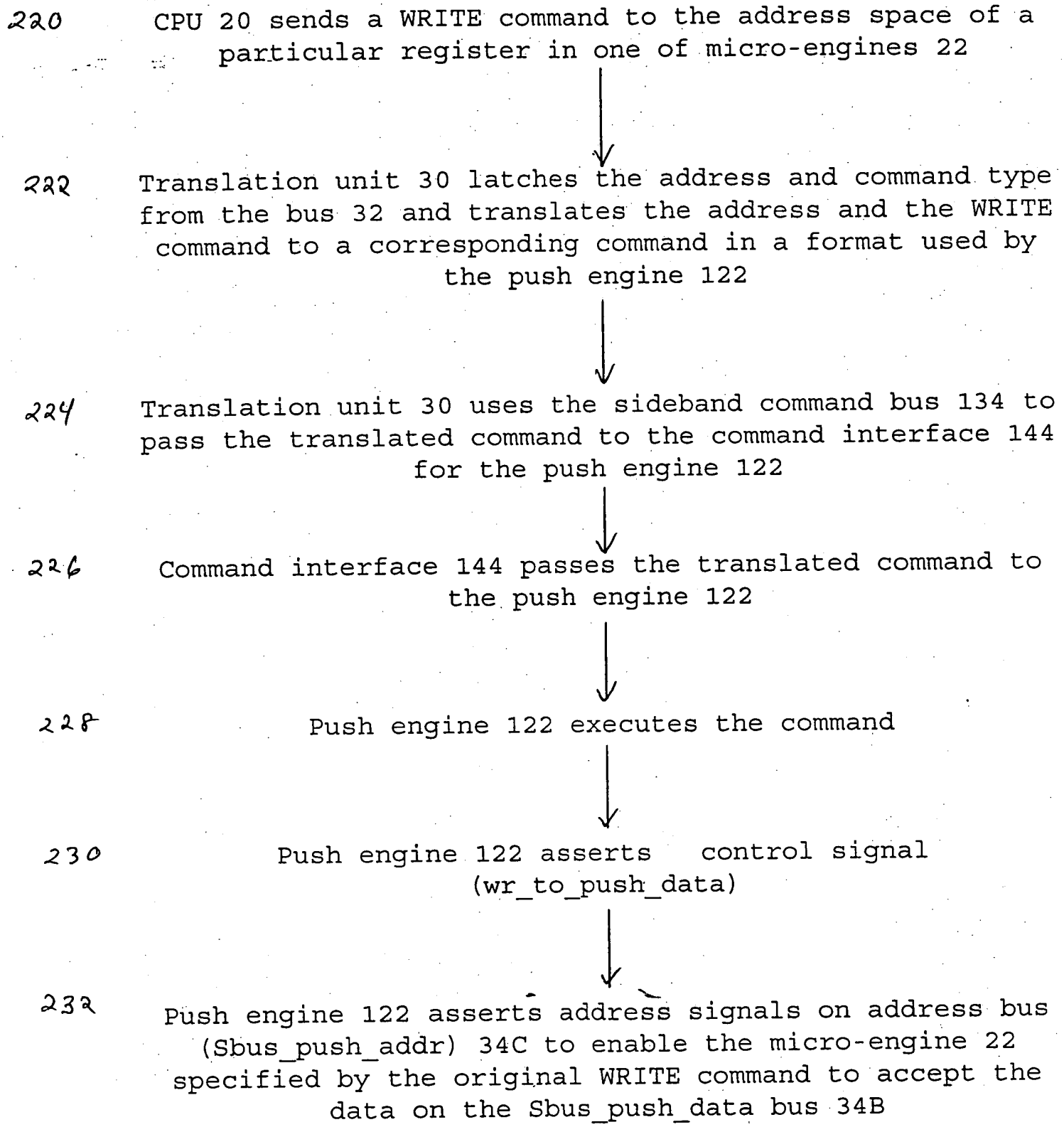


FIG. 6

240 CPU 20 sends a READ command to the address space of the particular destination in the FBUS interface

242 Translation unit 30 latches the address and command type from the bus 32 and translates the address and READ command to a corresponding command in a format that simulates the format used by the push engine 122

244 Translation unit 30 uses the sideband command bus 134 to pass the translated command to the command interface 144 which passes the translated command to the push engine

246 Push engine 122 executes the READ command to place the data from the FBUS interface destination that was specified in the READ command onto the Sbus-Push_data bus 34B

248 Push engine 122 asserts control signal (rd_from_push _data) on the bus 136

250 Translation unit 30 promotes the data from the bus 34B to the core processor bus 32 so that the data can be received by the CPU 20

FIG. 7

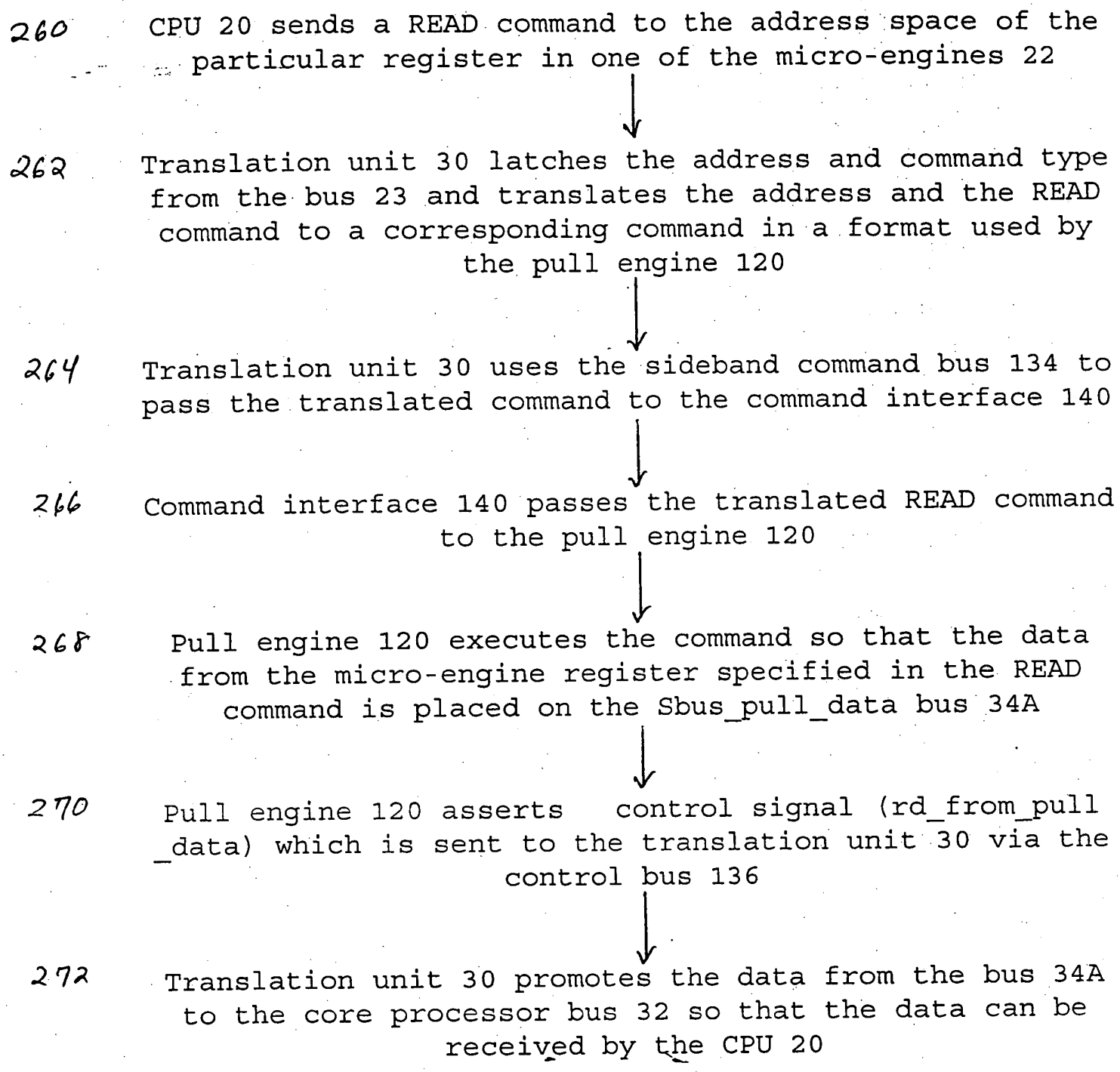


FIG. 8